11.2

(a)

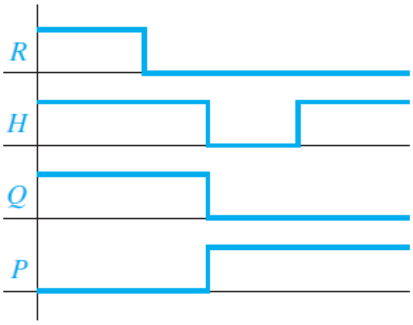
R = 1 and H = 0 cannot occur at the same time.

(b)

R	H	Q	Q^+
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	X
1	0	1	X
1	1	0	1
1	1	1	1

$Q^+ = R + HQ$

(c)

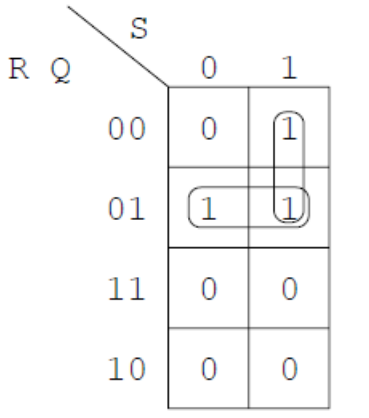


11.4 See p. 752 in the textbook

11.6

(a)

$S\,R\,Q$	Q^+
0 0 0	0
0 0 1	1
0 1 0	0
0 1 1	0
1 0 0	1
1 0 1	1
1 1 0	0
1 1 1	0



$Q^+ = R'Q + S\,R'$

(b) See p. 752 in the textbook

11.9 See p. 753 in the textbook

11.12

For circuit (a) and (b),

When S = R = 1, in (a), both outputs are 1, and in (b), the latch holds its state.

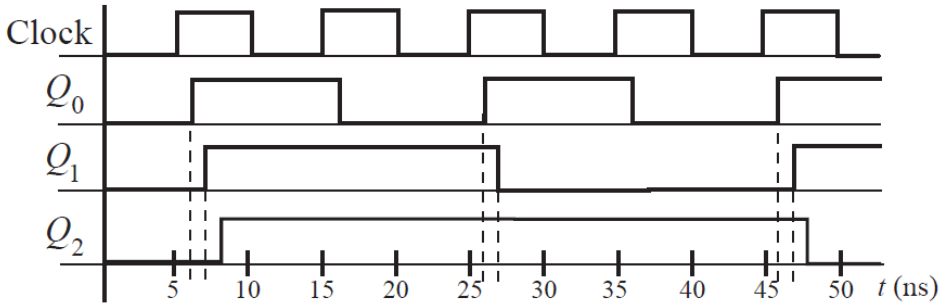
When S = R = 0, both Q in (a) and (b) will holding it's state.

When S = 0, R = 1, both Q in (a) and (b) will be set to 0.

When S = 1, R = 0, both Q in (a) and (b) will be set to 1.

S	R	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1

11.24



11.26